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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/501,493	02/09/2000	John Marland Garth	ST9-99-130	3937

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EXAMINER
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ART UNIT	PAPER NUMBER
2127	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/501,493	GARTH ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,20-30 and 39-49* is/are rejected.

7)☒ Claim(s) *12-19,31-38 and 50-57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action in response to application filed on February 9, 2000. Claims 1-57 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 20, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al. (US Pat 5,202,987) in view of Tsuchida et al. (US Pat 6,026,394).

Regarding **claims 1, 20, and 39**, Bayer et al. disclose a method of loading data into a data store connected to a computer, the method comprising the steps of:

identifying memory constraints (col. 1, lines 13 – 15, memory and processors are operations bottleneck and col. 5, lines 52 – 56, memory is constrained or limited through factors such as physical shared storage, network access or processor distribution, and common memory space);

identifying processing capabilities (col. 1, lines 17 – 27, synchronization activities are controlled by algorithm, which depends on processing power and col. 5, lines 24 – 31 requires the number of processors and capabilities of each processor, which entail processing capabilities); and

determining a number of load (col. 14, lines 25 – 33, loading capacity being part of task map) to be started in parallel based on the identified memory constraints and processing capabilities (col. 7, lines 9 – 1).

Although Bayer et al. disclose the sort process being a mere tasks allocation to the processors (col. 1, lines 44 – 50), Tsuchida et al. have nevertheless further detailed the sort feature, which includes the step of determining a number of sort processes (col. 8, lines 50 – 51 disclose the fact that the sorting process depends on the number of node for join process. Col. 7, lines 54 – 57 show that the number of join nodes for performing merge process can be determined. Hence, number of sort processes is a known quantity).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the sorting feature shown by Tsuchida et al. to the invention of Bayer et al. so that sort processing time, which is a factor in load balancing processes can be determined as part of system characteristics and optimization purposes (col. 7, lines 58 – col. 8, line 35). Note that the sort steps shown by Tsuchida et al. are also parallel processes as claimed in the application (fig. 3, parallel pipeline operation).

4. Claims 1, 20, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000).

As per **claims 1, 20, and 39**, Bhattachary et al. disclose a method of loading data into a data store connected to a computer, the method comprising the steps of:

identifying memory constraints (col. 9, lines 6 – 7, memory becomes a constraint as its capacity is a contributing factor and is limited);

identifying processing capabilities (fig. 1, number of processors p, col. 4, line 41 – col. 5, line 8, each processor is assigned with a specific number of tasks, hence indicating each limited capability); and

determining a number of load (col. 3, lines 1 – 3, join column domain and tuples are the load, which obviously much be known in order for them to be partitioned and transferred among the cluster, col. 3, lines 7 - 18), and sort processes (col. 2, line 62 – col. 3, line 6 disclose various method of parallel sort process in which merge join is one example. Since the actual tasks assigned to the processors are determined during the join phase, which is part of the sort process as shown above, number of sort processes are hence inherently determined as well) to be started in parallel based on the identified memory constraints and processing capabilities (col. 1, lines 24 – 28, parallel tasks based on processing capabilities: col. 4, line 64 – col. 5, line 8, parallel sort processing: col. 2, lines 66 – col. 3, line 6).

5. Claims 2 – 3, 21 – 22, and 40 - 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000) as applied to claims 1, 20, and 39 above and in view of Hintz et al. (US Pat 5,222,235).

Regarding **claim 2**, although Bhattacharya et al. did not clearly teach the method of claim 1 further comprising determining a number of build processes based on the number of sort processes, nevertheless, this teaching is considered common knowledge in the art per Hintz's invention (col. 5, lines 50 – 51). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize this common feature shown by Hintz et al., to the invention of Bhattacharya et al., as one in the pertained art would know that build process is a consequential step directly dependent on sort process.

Regarding **claim 3**, though Bhattacharya et al. taught the method of claim 1, except wherein the number of sort processes does not exceed a number of indexes to be built, nevertheless, according to the disclosure of Hintz et al. (as cited in grounds for rejection of claims 2, 21 and 42), "one index at a time" clearly indicates the claimed invention, in which the number of indexes excessive to the number of sort processes would not be possible. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate this feature disclosed by Hintz et al., to the invention of Bhattacharya et al. so that the number of build indexes can not exceed the number of sort processes.

Claims 21 – 22 and 40 – 41 are rejected on the same ground as stated above.

6. Claims 4 – 6, 23 – 25, and 42 - 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000) as applied to claims 1, 20, and 39 above and in view of Bordonaro et al. (US Pat 5,307,485).

Regarding **claim 4,** though Bhattacharya et al. taught the method of claim 1, except wherein the number of load processes does not exceed a number of partitions to be loaded, nevertheless, this feature has been illustrated by Bordonaro et al. (fig. 3, 310 shows N partitioned tasks and 312 distributes over the N processors). In fig. 2, 202 shows that as the records from storage device are loaded, col. 4, line 62 – col. 6, line 27 describes the fact that N partitioned tasks corresponds to N processors, which implies the limitation, in which the number of load processes does not exceed a number of partitions to be loaded. Note that fig. 2 corresponds to fig. 3 in that records loaded into memory are to be part of the portion from which tasks are created (col. 5, lines 58 – 60) and subsequently, divided in to partitions for load processes, as shown in fig. 3. Therefore, it would have been obvious to one of ordinary skill in the art, at the

time the invention was made, to integrate the feature disclosed by Bordonaro et al. to the invention by Bhattacharya et al. so that various memory constraints would still be suitable to apply the desired processes (col. 1, lines 33 – 56).

Claim 5 is rejected based on the indicated rational above since Bordonaro et al. comprehensively taught both load (described above) and sort processes (col. 1, lines 57 – 68), which are then processed by the N processors. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize the advantage of combining the features disclosed by Bordonaro et al. to the invention of Bhattacharya et al. for overall efficiency purposes.

Regarding **claim 6**, although Bhattacharya et al. taught the method of claim 1, except wherein the memory utilized by the load and sort processes does not exceed memory constraints, nevertheless, Bordonaro et al. shows the load and sort processes directly dependent on memory constraints (col. 5, lines 54 – 62). Therefore, this is considered obvious to one pertaining an ordinary skill in the art, to recognize that, in designing computer system to load data, in which balancing the loads become an issue, to take into account the memory constraints.

Claims 23 – 25, and 42 – 44 are rejected on the same ground as stated above.

7. Regarding **claims 7 – 11, 26 – 30, and 45 – 49**, the examiner takes an Official Notice that the limitations narrowed by these claims are considered obvious and furthermore a matter of design choice, since applicants have not disclosed that the claimed limitations solve any stated problem or are for any particular purpose and it appears that the invention would perform equally well without the claimed features. Therefore, it would have been obvious to one of ordinary skill

in the art, at the time the invention was made, to efficiently utilize all the processing capabilities required for the desired task.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 20 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Garth et al. (US Pat 6,272,486 B1).

Regarding **claims 1, 20, and 39**, Garth et al. disclose a method of loading data into a data store connected to a computer, the method comprising the steps of:

identifying memory constraints (col. 1, lines 53 – 55);

identifying processing capabilities (col. 4, lines 14 – 17); and

determining a number of load (col. 1, lines 56 – 57, indices built indicates known number of load, col. 5, col. 1 – 10 shows a known number of extract tasks N_u), and sort processes (col. 5, lines 42 – 52 and col. 6, lines 61 – 67) to be started in parallel based on the identified memory constraints and processing capabilities (col. 4, lines 17 – 26).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37

CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Allowable Subject Matter

10. **Claims 12 – 19, 31 – 38, and 50 - 57** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is (703) 305-7864.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Lilian Vo
Examiner
Art Unit 2127

lv
April 17, 2002